San Jose State University

Department of Aviation/Technology

College of Engineering

Tech 63: Digital Circuits	Kenneth Cole
IS 216 Lec: Tuesday 3:00 PM to 4:45 PM	Office: IS 117
IS Labs Either Tues 5:00 PM or Thur 3:00 PM	During Lab sessions
Kenneth.cole@sjsu.edu	PH :(650) 224 6458

The class will start with the first lecture on 1/31/17 Tuesday and the first lab will follow the lecture. The repeat section for the Lab will be held on Thursday, 2/2/17. Students will be expected to enroll in one of the lab sections and stick to this enrollment for the duration of the course. You will be in self-selected lab teams and will work together and hand in a single report for the team. Should these lab periods not be reasonably balanced, students will be asked to transfer to the other lab from the overpopulated lab. **Note that classes start on Thur 1/26/17 but we will not start the lab at that time as we will not have had our first organization lecture. So, no lab on 1/26/17.**

Course Description

Logic gates emphasizing TTL and CMOS. Design techniques. Combinational circuits, counters, registers, multiplexers, de-multiplexers, encoders, decoders, and logic gates. Course will include familiarization with digital programming of FPGAs

Prerequisite: Tech 60

Textbook

Floyd, Thomas L., **Digital Fundamentals**. 11th Edition. Upper Saddle River, New Jersey: Prentice Hall, 2003

Lab Manual

Buchla and Joksch Experiments in Digital Fundamentals, eleventh edition lab manual

Course Objectives

Upon successful completion of this course, the student will have:

1. Understand the principles of single logic gate devices and serial manipulation of logic streams.

2. Comprehend the working knowledge of flip-flops and related devices.
3. Describe counters and registers.
4. Understand interfacing with the analog world.
5. Explain the operations of encoders, decoders, multiplexers and De-multiplexers.
6. Comprehend manipulation of digital streams of data using Programmable Logic Devices and codes such as VHDL

Course Evaluation

Midterms

Midterm #1 and # 2	20%	200
Quiz	10%	100
Lab(13 labs)	30%	300
Homework	12%	120
Final	28%	280
Total	100%	1000

Final:

Grading

The final grade will be determined according to the following scale:

A+	97 -100%	B+	87 - 89%	C+	77 - 79%	D+	66 - 69%
A	93 - 96%	B	83 - 86%	C	73 - 76%	D	60 - 65%
A-	90 - 92%	B-	80 - 82%	C-	70 - 72%	F	00 - 59%

I. Examinations & Quizzes

There will be two examinations given during the semester.
Unexcused absences will lead to a zero grade.

There will be one quizzes given during the semester.
The quiz will be unannounced and broken into multiple segments so that it does not interfere with the lecture planned. Quizzes will most likely be administered during Lab periods.
Unexcused absences will lead to a zero grade.

II. Homework Assignments

You will be assigned a certain number of problems weekly, and told what date the problems are due. Sufficient time will be given to complete each assigned homework set. Remember, the assigned homework must be submitted on the assigned due date. Late homework will be accepted but penalized. Please note, Canvas will consider a missing assignment as a zero after the deadline for submission is past. Since HW can be turned in late, this has the effect of making students think their final grade is higher than it will be at the end of the term. This will not be accepted as a reason to change or alter a student's grade after the final deadline for assignments is complete, this is usually the day of the final exam or sooner if announced. Treat unfinished assignments as zero unless other arrangements are made. Canvas will be instructed to count unentered assignments as zero for final grade determination.

Academic Integrity Policy:

Your own commitment to learning, as evidenced by your enrollment at San Jose State University, and the university's Academic Integrity Policy requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the Office of Student Conduct and Ethical Development. The policy on academic integrity can be found at http://sa.sjsu.edu/student_conduct.

Americans with Disabilities Act Policies:

If you need course adaptations or accommodations because of a disability, or if you need special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours.

Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with DRC to establish a record of their disability.

Experiment write-up Format

A written laboratory report for each experiment is required. The report should contain the following components:

Cover Page: This page includes the title of the experiment, the date, the course number, the course name, and each team member's name. The inclusion of a student's name on the report signifies that the student took part in the lab and shared in the work effort.

Objective: The objective tells what the experiment is all about. Write short sentences to explain the reasons for doing the experiment. When circuits are provided, add the circuit to the objective to make the procedure clear.

Equipment: Write down the equipment and the components used for the experiment

Procedure: Write down the steps in a logical sequence to do the experiment.

Theory: The solution to the expected problem should exemplify the theory with calculations. All steps must be clarified with circuit diagrams. After you have solved the problem your next step will be to make a table showing all the parameters to be verified when you do the actual experiment. In other words, you simply want to verify your theoretical results or calculations in the laboratory.

Data: Your data must represent the experimental results.

Conclusion: The conclusion tells what you accomplished by doing the experiment. In other words, did the experimental results agreed with your expected results? Write a full faith explanation of the results even if the whole experiment was not finished or the results did not conform to the theory. If possible indicate what troubleshooting was done to investigate unexpected results.

General Comments: The report must be neat, legible, and double spaced, and submitted in a type written form (use your computer). Use simple sentences that get right to the point. Be specific! Use 8 ½ x 11 inch paper with **no holes** or **perforated edges**. Staple all of the pages together at the upper left-hand corner. **Do not tear** or **fold** the corners!

General Laboratory Grading per Experiment

	Points
1. Objective & Circuits	2
2. Equipment Listing	1
3. Theory	5
4. Procedure	5
5. Data	5
6. Conclusion	5
Total points	23

Tentative Calendar

Week of	Lecture Topics	Problems
01/31/2017 Week 1	Green Sheet, Lab Procedures Chapter 1	Odd problems Ch 1 (1 – 20) Lab # 1
02/07/2017 Week 2	Ch 1 Continued	Ch 1 Odd Problems (21 – 43) Lab # 2
02/14/17 W3	Ch 2	Odd numbered problems (1-33) Lab # 3
02/21/17W4	Ch 2 Continued	Odd numbered problems (34 – 69) Lab # 4
02/28/16 W5	Ch 3	Odd numbered problems (1-25) Lab 5
03/7/17 W6	Ch 3 Continued	Odd Numbered problems (26 – 55)

	Review for Midterm	Lab 6
03/14/17 W7	**Midterm 1**	Lab 7
03/21/17 W8	Ch 4	Odd numbered problems (1-36) Lab 8
04/4/17 w 9	**Ch 4 Continued)**	Odd numbered problems (37-72) Skip Karnaugh subject problems Skip Applied Logic display problems Include VHDL problems Lab 9
4/11/17 W10	Ch 5	Odd numbered problems (1-25) Lab 10
4/18/17 W11	Ch 5 Continued Review for Midterm 2	Odd Numbered problems (26-51) Lab 11
04/25/17 W12	Midterm 2	Lab 12
05/2/17W13	Ch 6	Odd numbered problems 1 – 33) Lab 13
05/9/17 w 14	**Ch 7**	Odd numbered problems (1 – 37) Make up for Unfinished Labs
5/16/17	**Review for Final**	Make up for Unfinished Labs Final deadline for turning in assignments; labs, Homework, Etc.

5/18/2017	**Final Exam** **1445-1700**	http://info.sjsu.edu/static/catalog/final-exam-schedule-spring.html

Subject to change with fair notice

Tentative List of Experiments

Lab#1 Lab Instrument Familiarization

Lab#2 Constructing a Logic Probe

Lab#3 Number Systems

Lab#4 Logic Gates

Lab#5 More Logic Gates

Lab#6 Interpreting Manufacturing Data Sheets

Lab#7 Boolean Theorems and De Morgan's Theorems

Lab#8 Logic Circuit Simplification

Lab#9 Perfect Pencil Machine

Lab#10 Experiment 11 Adder and Magnitude Comparator

Lab#11 Experiment 12 Combinational Logic Using Multip0lexers

Lab#12 Experiment 13 Combinational Logic Using Demultiplexers

Lab#13 Experiment 14 The D Latch and D Flip Flop