San José State University
Department of Aviation &Technology
Tech 63 Analog and Digital Circuits, Spring 2018

Course and Contact Information

Instructor:	Dr. Pouya Ostovari
Office Location:	IS 106
Telephone:	(408)-924-3917
Email:	pouya.ostovari@sjsu.edu
Office Hours:	MW: 14:00 – 15:00 or by an appointment
Class Days/Time:	MW: 12:00 – 12:50 Lecture M: 15:00 – 17:45 Lab
Classroom:	Lectures: Engr. 103 Lab: IS 117

Prerequisites:
Tech 60

Course Format

The course relies on lecture and lab materials presented in class and students are strongly encouraged to attend and participate in the discussions.

Course Description

Logic gates emphasizing TTL and CMOS. Design techniques. Combinational circuits, counters, registers, multiplexers, Semiconductor theory. Operational amplifiers. Device applications, signal generators, voltage regulators and power supplies.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

1. Build, test and troubleshoot combinational logic circuits.
2. Design, build and troubleshoot counters, registers, multiplexers, and memory devices
3. Explain the interfacing between the digital and analog world.
4. Describe the fundamentals of semiconductors, op-amps, timers, power supplies and oscillators.

5. Design, build and troubleshoot diode circuits, transistor circuits, op-amp circuits, active filters, and oscillators.
6. Design or modify fundamental electronic circuits to meet certain requirements.

Required Texts/Readings

Textbook

1. Floyd, Thomas L., Digital Fundamentals. 11th Edition, Upper Saddle River, NJ: Prentice Hall, 2014.
2. Floyd, Thomas L., Electronic Devices Conventional Current Version. 9th Edition. Upper Saddle River, NJ: Prentice Hall. 2012.

Course Requirements and Assignments

You will answer selected questions for each chapter. Homework and lab assignments will be posted on Canvas. You should submit your work via Canvas by the due date.

Final Examination

The final exam will be comprehensive, covering all material presented in class.

Grading Information

Homework	10%
Quizzes	10%
Midterm 1	15%
Midterm 2	15%
Lab	25%
Final Exam	25%

The final grade will be determined according to the following scale:

A+ 96-100	B+ 87-89	C+ 77-79	D+ 67-69	F <60
A 93-95	B 83-86	C 73-76	D 63-69	
A- 90-92	B- 80-82	C- 69-72	D- 60-62	

1. Check continuously your standing in the class on Canvas (https://sjsu.instructure.com). Notify the instructor immediately if there is an error in any of your grades.

2. All late assignments submitted up to 7 calendar days after the due date and time will have a penalty of 10% per day.

3. **Assignments submitted after 7 calendar days of the due date will not be accepted and they will be recorded as 0.**

4. There will not be any makeup quiz, but your lowest quiz grade will NOT be considered.

Classroom Protocol

Class participation and attendance are strongly encouraged. Use of cell-phones are not allowed. Laptop computers and tablet are allowed only for taking lecture notes and related work to the lectures.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

Students with Special Need

If you need special accommodation, please contact Accessible Education Center at your earliest convenience. You can find more information at http://www.sjsu.edu/aec/faculty/index.html.

Tech 165 Wireless Communications Technologies, Fall 2017 Course Schedule/Outline

Tentative Calendar*

Week	Topics, Readings, Assignments, Deadlines
1, Jan 24th	• Introduction, Green Sheet, Course Organization, Orientation • Chapter 1 (*Introductory Concepts*)
2, Jan 29th	• Chapter 1 continued - Chapter 2 (*Number Systems, Operations, and Codes*)
3, Feb 5th	• Chapter 2 continued
4, Feb 12th	• Chapter 2 continued
5, Feb 19th	• Chapter 3 (*Logic Gates*)
6, Feb 26th	• Chapter 4 (*Boolean Algebra and Logic Simplification*)
7, Mar 5th	• Chapter 4 continued • **Midterm exam 1**
8, Mar 12th	• Chapter 4 continued
9, March 19th	• Chapter 4 continued - Chapter 5 (*Combinational Logic Analysis*)
10, Apr 2th	• Chapter 5 continued
11, Apr 9th	• Chapter 6 (*Functions of Combinational Logic*) • **Midterm exam 2**
12, Apr 16th	• Chapter 1 (*Introductory to Electronics*) • Chapter 2 (*Diodes and Applications*)
13, Apr 23th	• Chapter 2 continued • Chapter 3 (*Special-Purpose Diodes*)
14, Apr 30th	• Chapter 4 (*Bipolar Junction Transistors*)
15, May 7th	• Chapter 5 (*Transistor Bias Circuits*)
15, May 14th	• Chapter 6 (*BJT Amplifiers*) • Chapter 7 (*Power Amplifiers*)
Friday, May 18	• **Final exam**, 12:15-14:30

* Subject to change with fair notice

Spring Break: Monday, March 26 - Friday, March 30

You can find the calendar at http://info.sjsu.edu/static/policies/calendar-fall.html